V5+_CORE　Modify list

RC00

2019-1-26 核对FMUV5管理图，进行细节修改

1：IO修改 PB6/PB7 将这些IO释放为普通GPIO使用，原来是POWER切换芯片的ABC检测
PB6=IO_SPARE_GPIO1,PB7=IO_SPARE_GPIO2,PB12=IO_SPARE_GPIO6

2019-1-28

1：修改板对板连接器，让定义分类更集中和规范

2：移动80P连接器位置，因为定义已不兼容，所以让结构上与之前的不兼容，避免误插问题

3：修改内部IMU扩展总线为SPI6，之前的为SPI5

RC01

2019-2-15

1：修改DSM&SBUS输出和PPM输入，让其分开为单独2个接口

2019-2-25

1：修改CAN芯片的S引脚上拉

2：修改了IST8310位置，避免TF卡槽导致罗盘干扰的问题

3：修改V5+的硬件ID

RC00

2019-1-26　Check the FMUV5 schematic to modify inconsistencies.
Modify the io PB6/PB7 pins.

2019-1-28

Modify the B_TO_B connector pins to make them more standardized.

Move the connector location so that it is not compatible with v5 (to prevent false connections.)

Modify the internal IMU expansion bus to SPI6 instead of SPI5

RC01

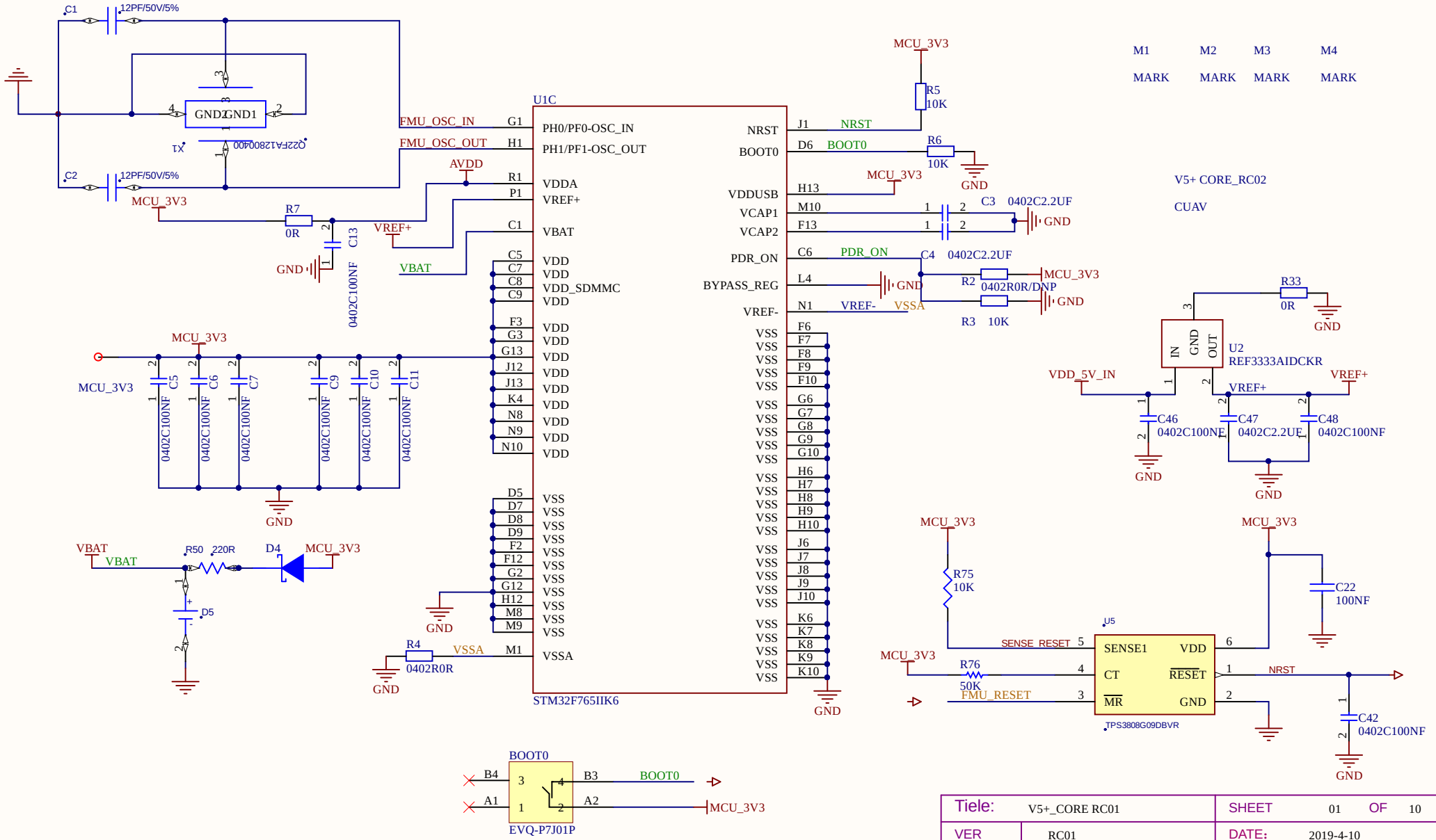
2019-2-15

1: Modify the DSM&SBUS output and PPM input to separate them into two separate interfaces

2019-2-25

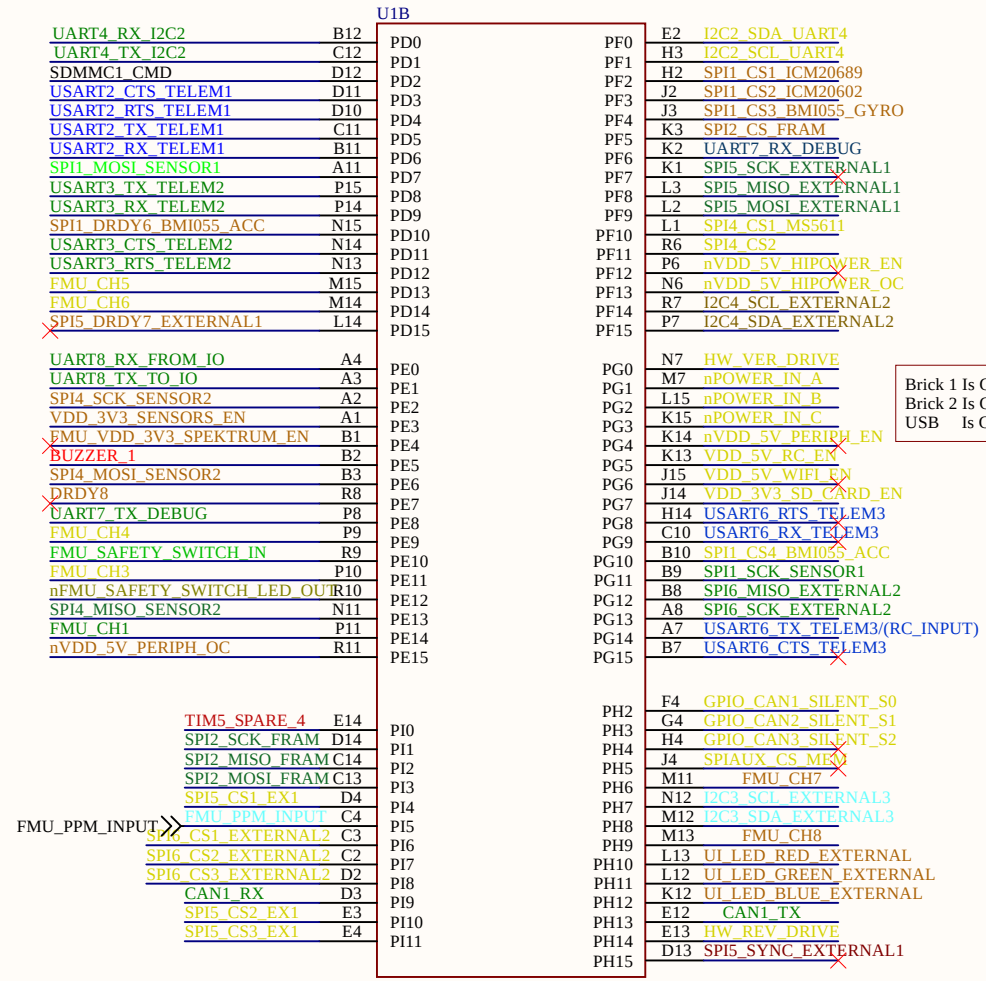
1: Modify the S pin pull-up of the CAN chip

System of STM32F765IIK6

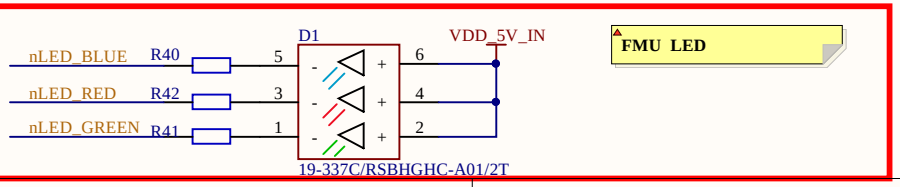


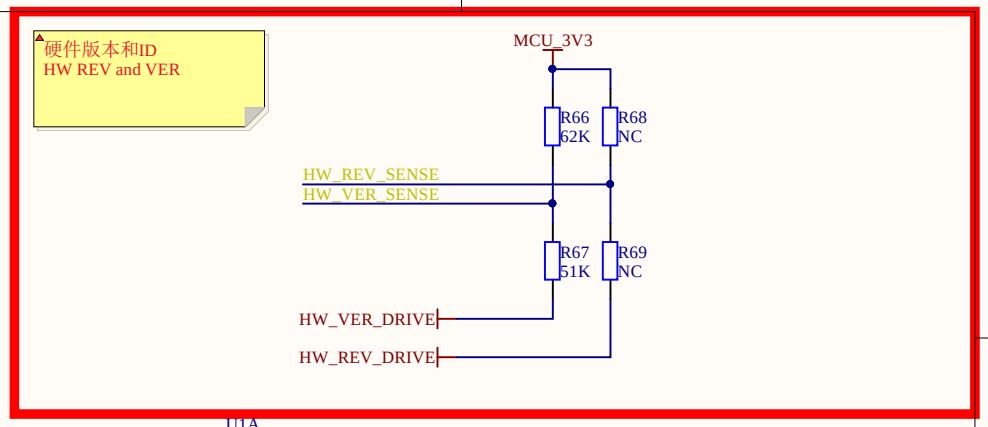
Tiele:	V5+_CORE RC01	SHEET 01 OF 10	
VER	RC01	DATE: 2019-4-10	
Designer	bin		
Reviewed			

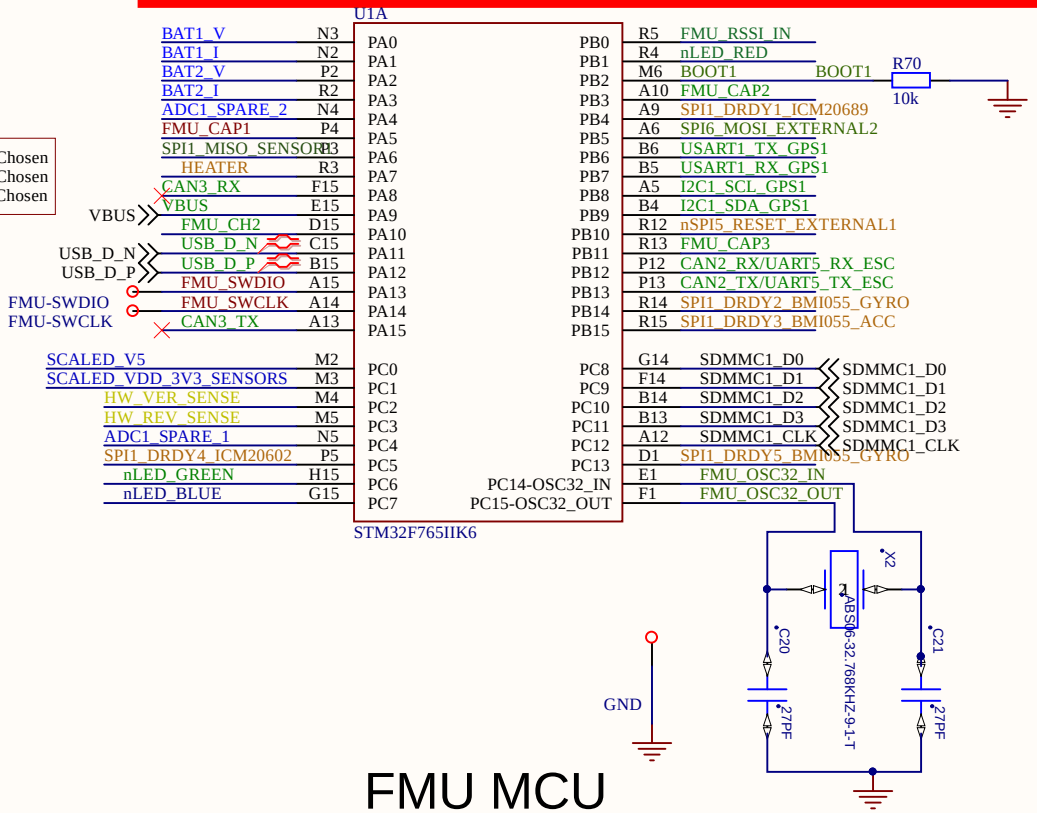
I/O of STM32F765IIK6



Brick 1 Is Chosen
Brick 2 Is Chosen
USB Is Chosen





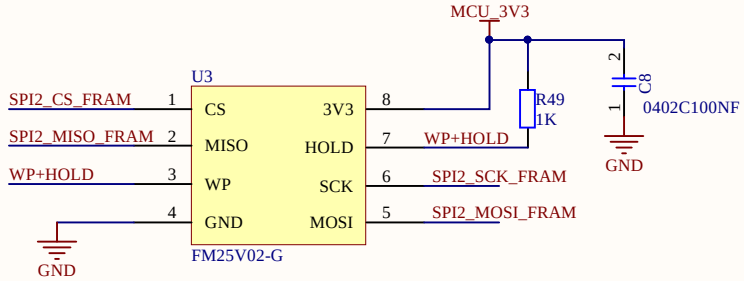


FMU MCU

Tiele:	V5+_CORE RC01	SHEET	02 OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

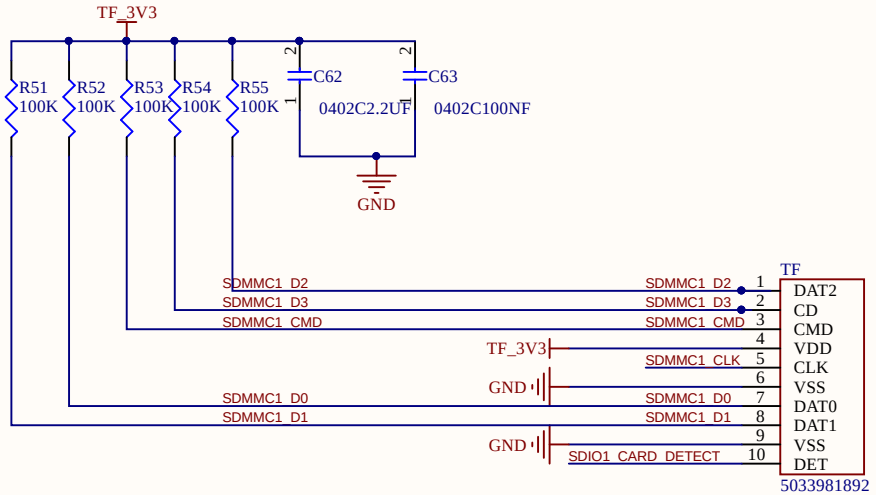
TF CARD + MTD of STM32F765IIK6

FRAM



FM25V01-G/FM25V02-G Compatible

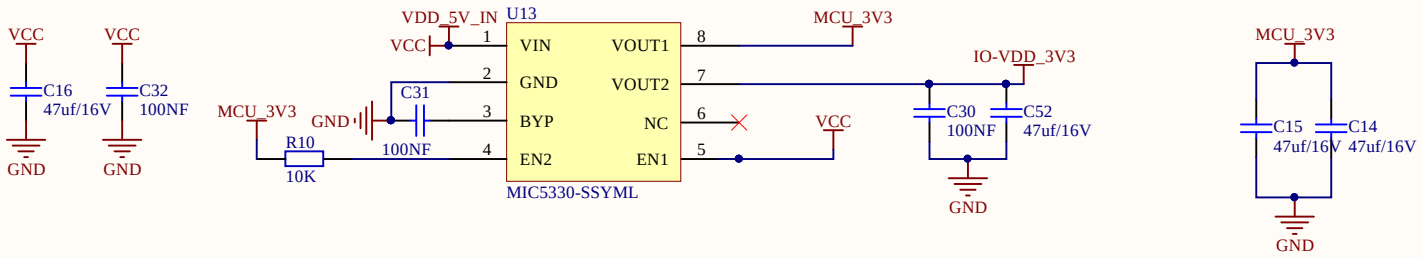
TF



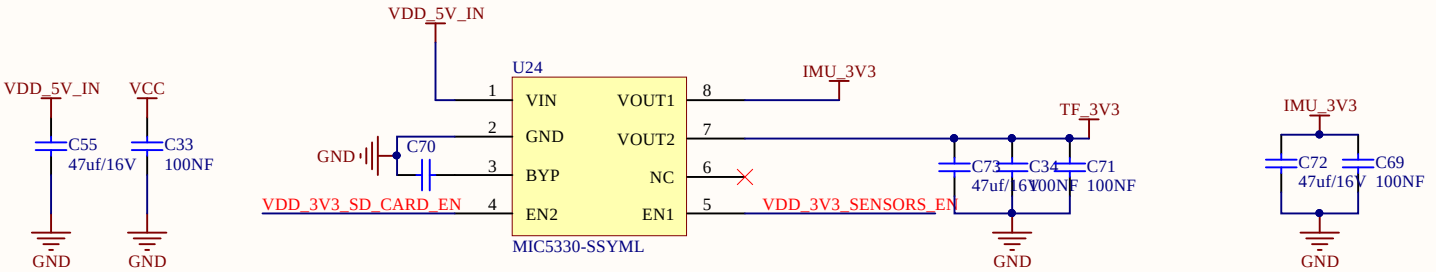
Tiele:	V5+_CORE RC01	SHEET	03 OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

LDO POWER

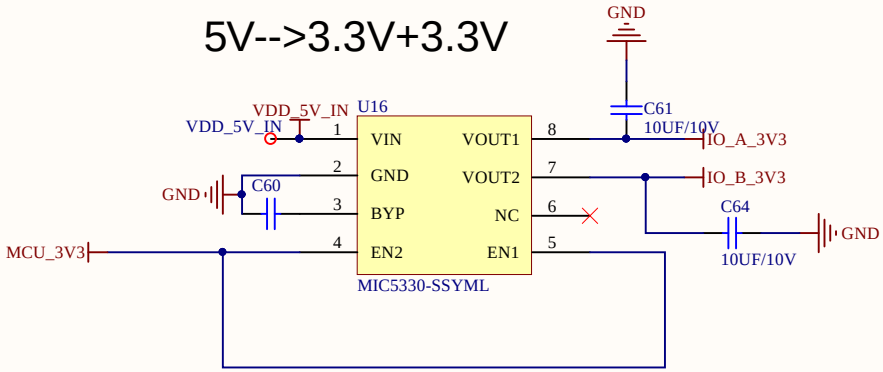
5V-->3.3V+3.3V



5V-->3.3V+3.3V



5V-->3.3V+3.3V



Power Startup sequence:

1:MCU_3V3

2:IO_A_3V3/IO_B_3V3/IO-VDD_3V3

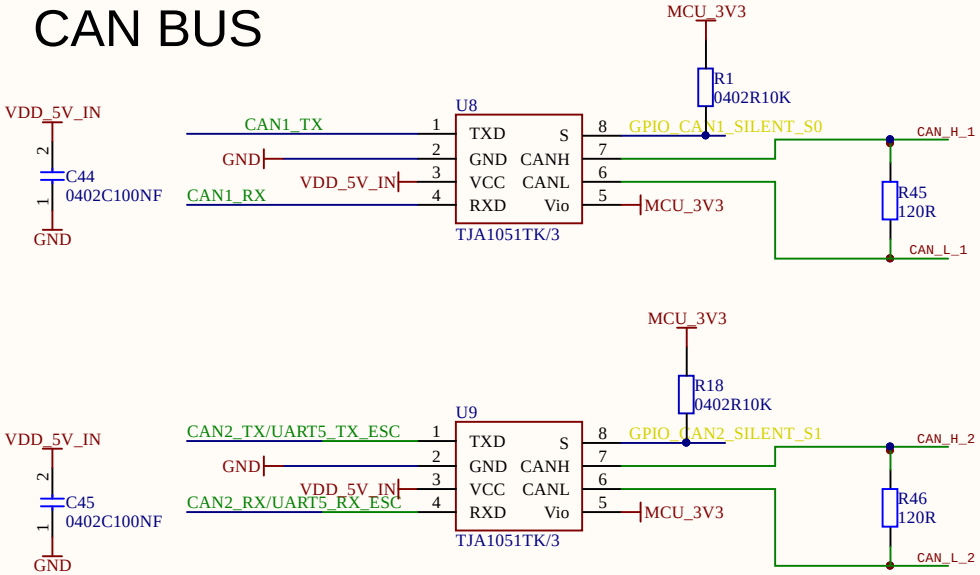
3:After the system starts successfully, it is turned on.

IMU_3V3 TF_3V3

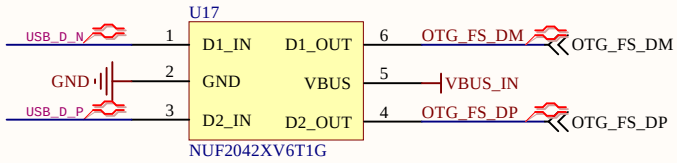
ALL POWER

Tiele:	V5+_CORE RC01	SHEET	05 OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

CAN BUS

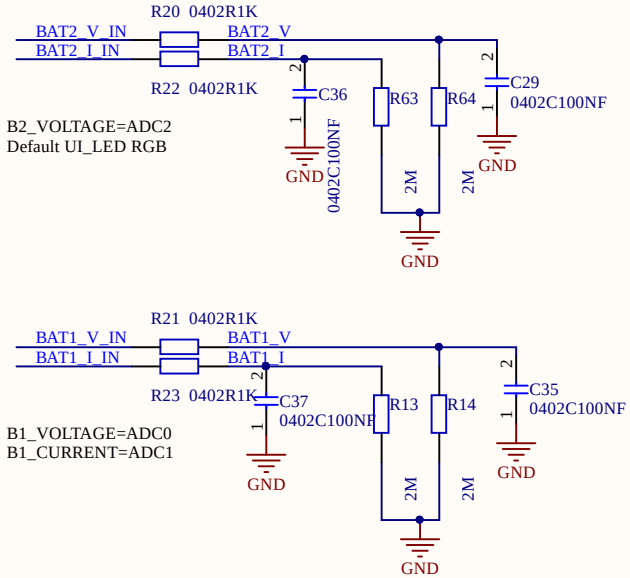


USB

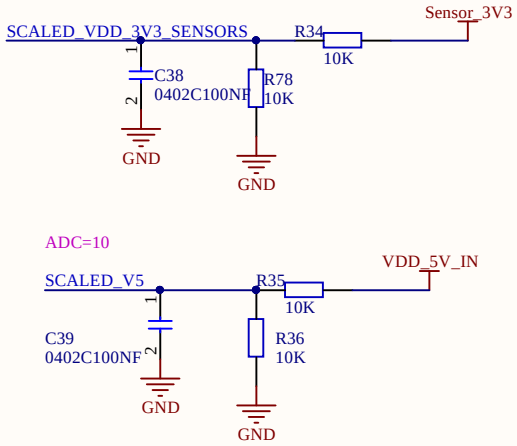


Tiele:	V5+_CORE RC01	SHEET	06 OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

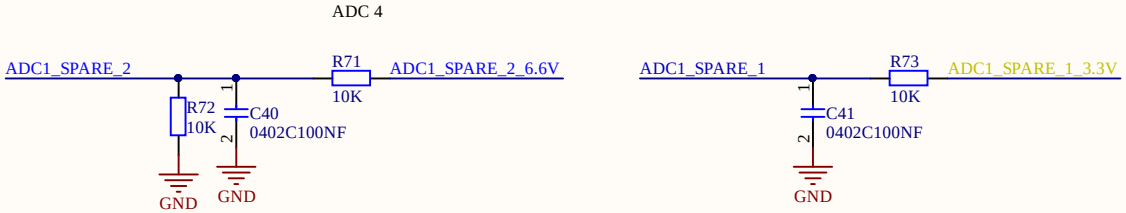
PM1 & PM2 voltage and current sensing



Core voltage detection



ADC of 3.3V + 6.6V



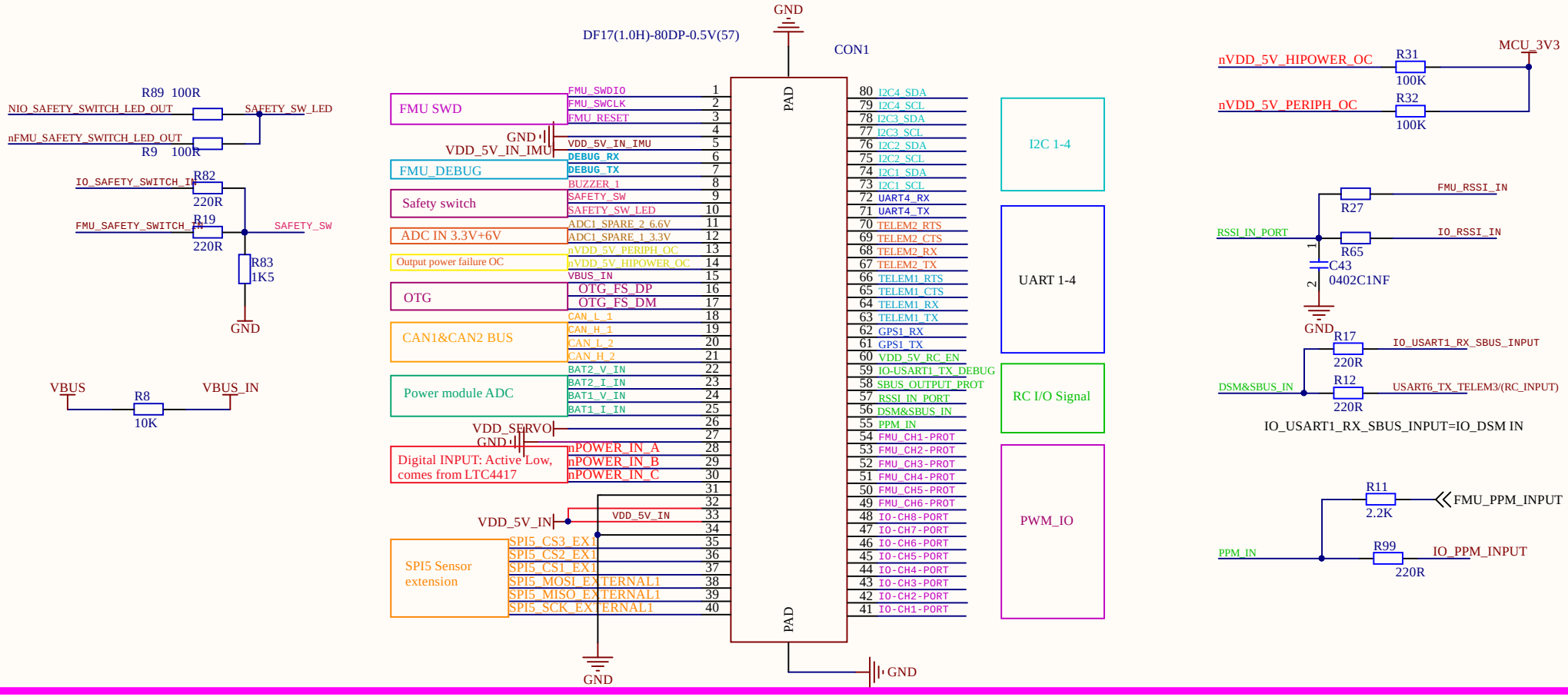
ADC IN

Tiele:	V5+_CORE RC01	SHEET	07 OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

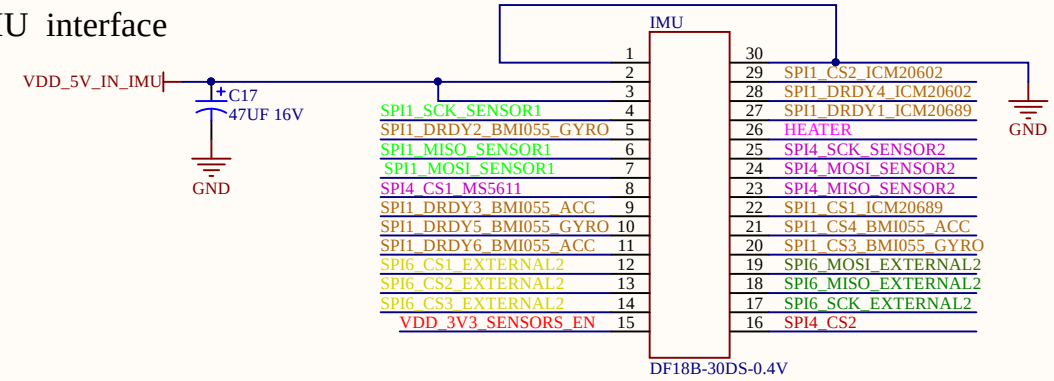
B_TO_B interface

80P板对板连接器定义只兼容CUAV V5+_CORE 标准，其他类似模块不能兼容

Only compatible with CUAV V5+_CORE module, other incompatible

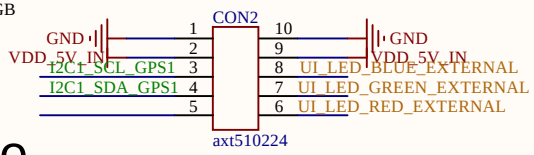


IMU interface



RGB interface

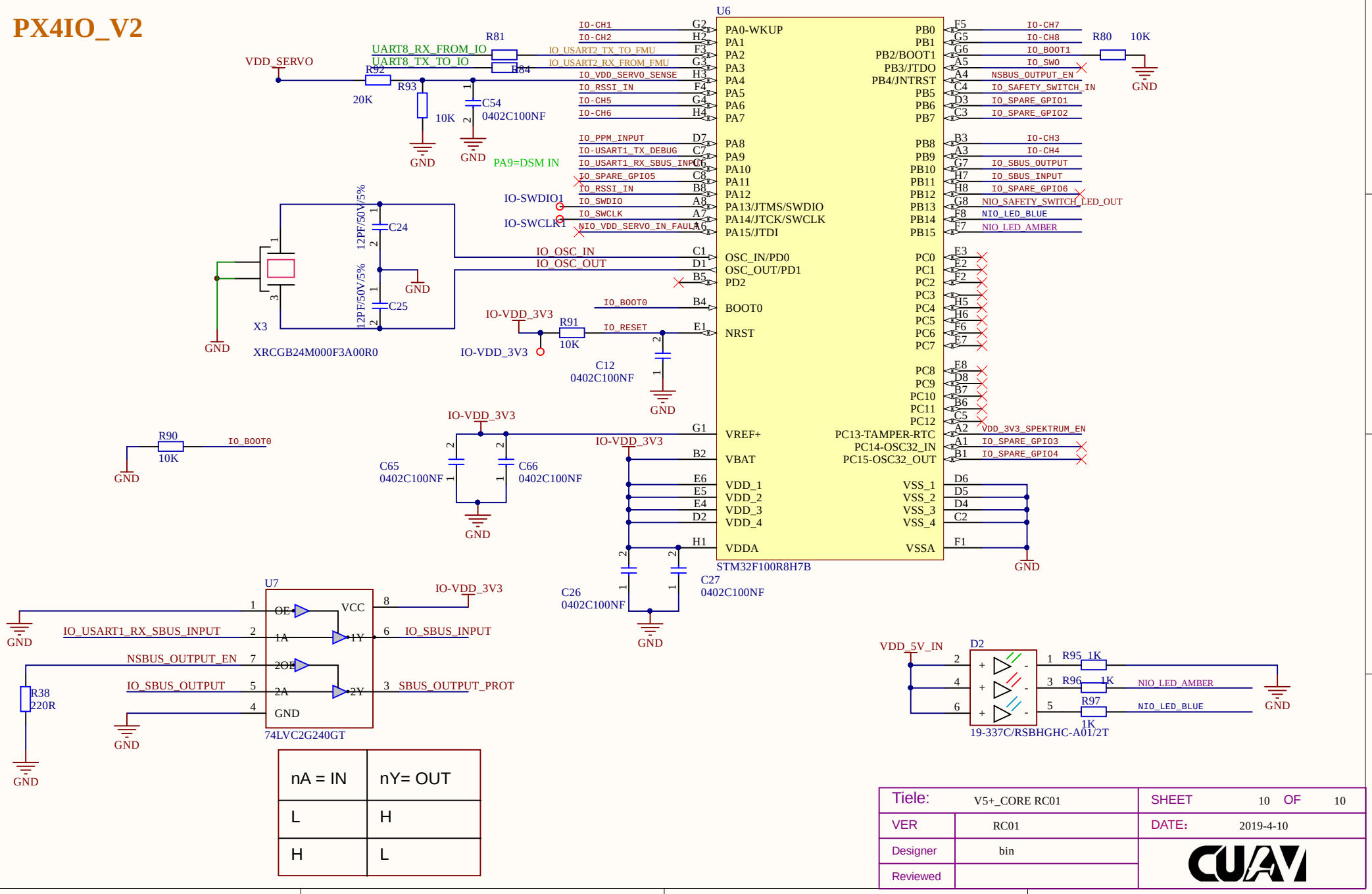
Default UI_LED RGB



Interface

Tiele:	V5+_CORE RC01	SHEET 08	OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

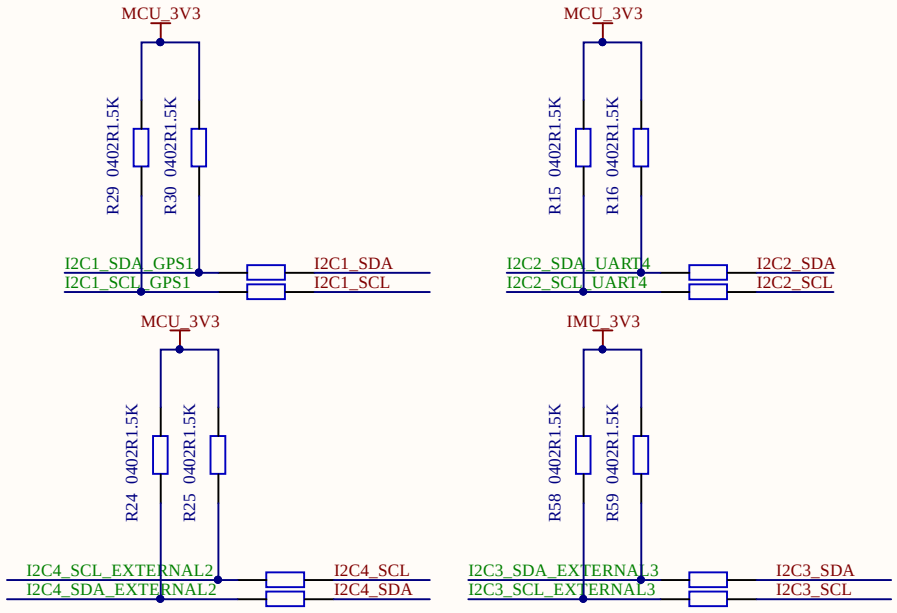
PX4IO_V2



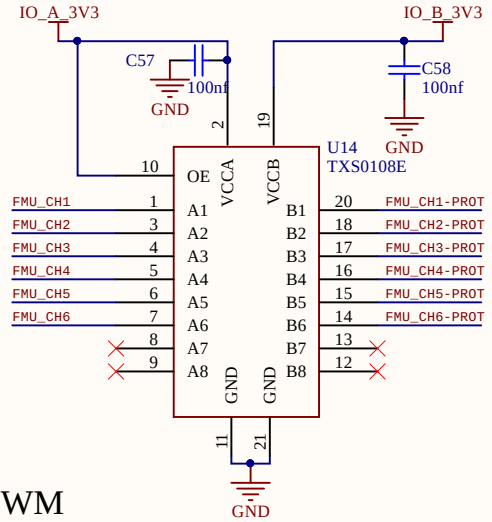
nA = IN	nY= OUT
L	H
H	L

Tiele:	V5+_CORE RC01	SHEET	10 OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

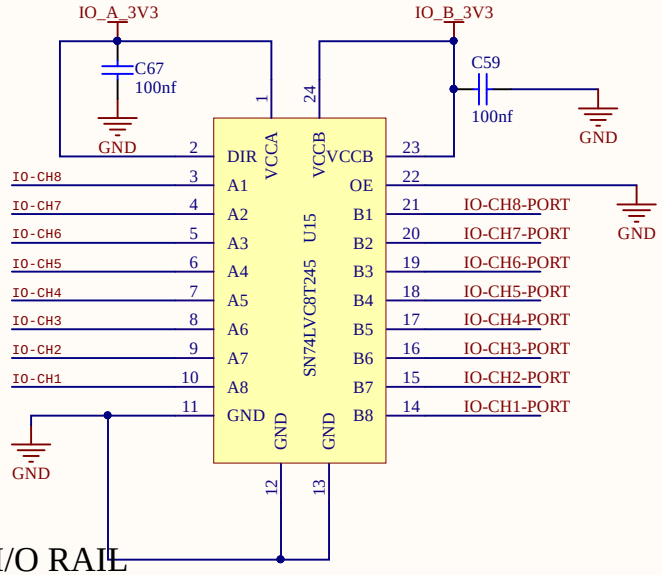
I2C



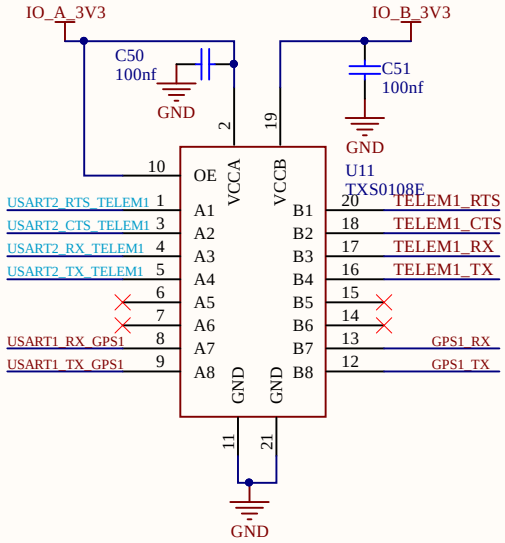
PWM

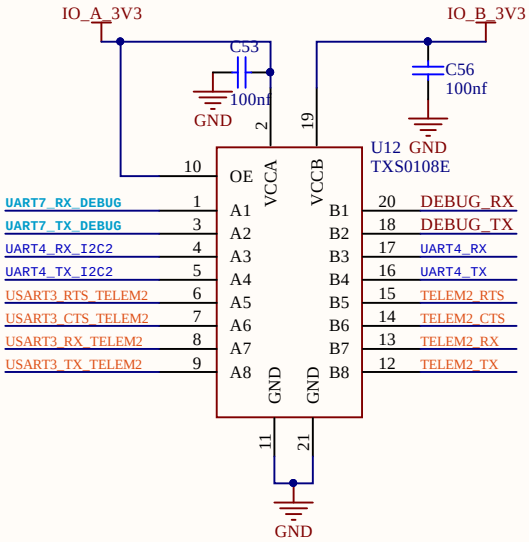


PWM



UART

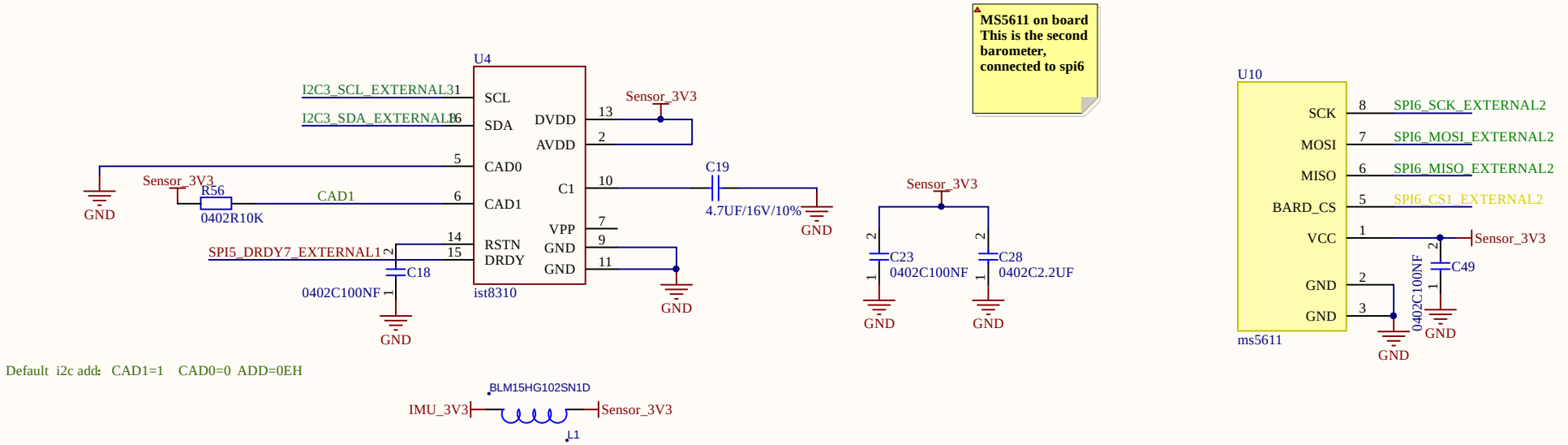




I/O RAIL

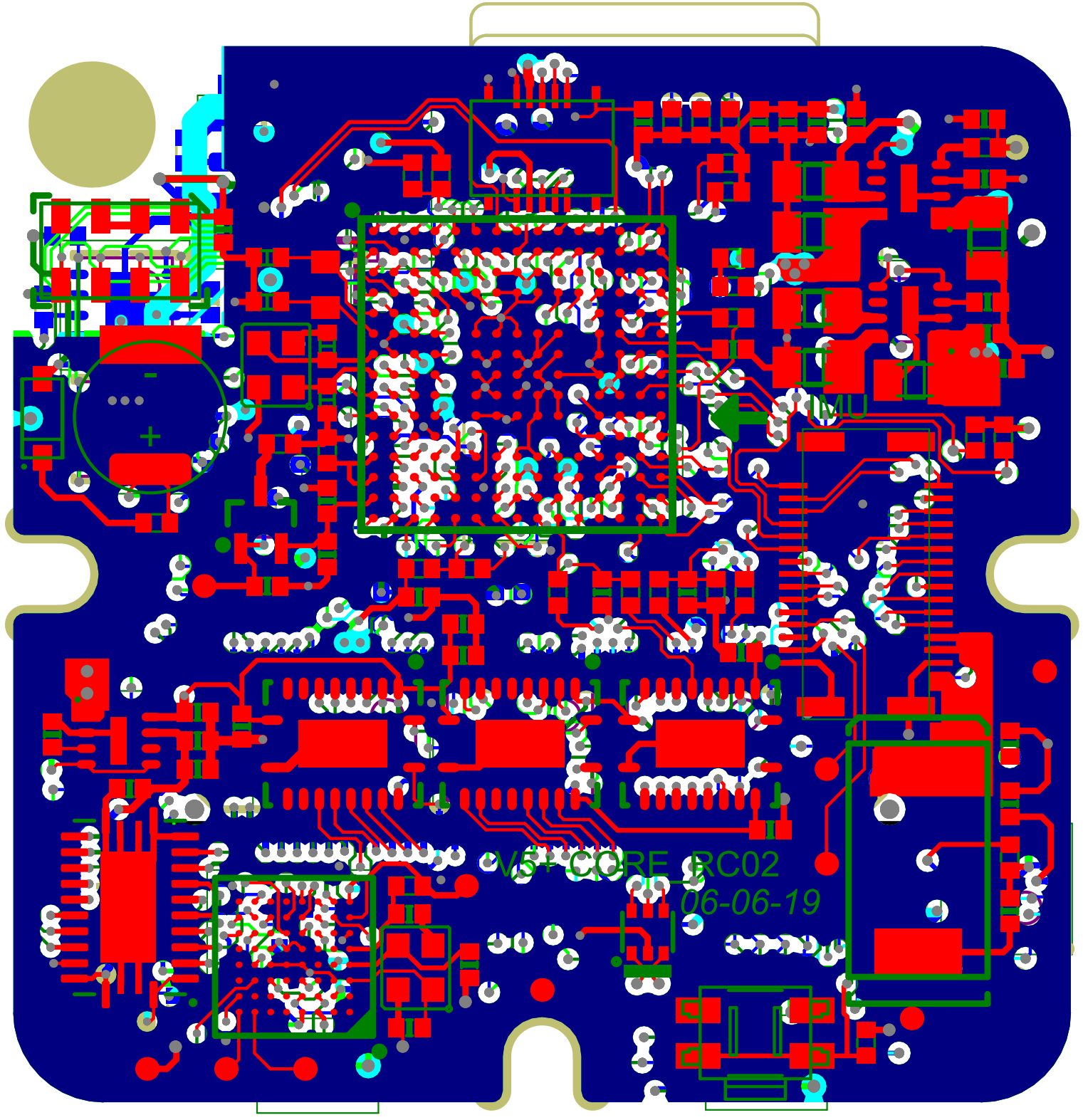
Tiele:	V5+_CORE RC01	SHEET 09	OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			

Sensor on board



CAN,USB,SENSOR

Tiele:	V5+_CORE RC01	SHEET	04 OF 10
VER	RC01	DATE:	2019-4-10
Designer	bin		
Reviewed			


V5+ CORE RC02
06-06-19